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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10091934	03/06/2002	716	/	2825	Levin

**APPLICANTS: Alon Amir; Goren David; Gordin Rachel; Livshitz Betty; Sherman Anatoly; Zelikson Michael;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed 35 USC 119 conditions met	<input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> yes <input type="checkbox"/> no	ATTORNEY DOCKET NO IL920020007US1
Verified and Acknowledged Examiner's initials		
TITLE : Interconnect-aware methodology for integrated circuit design		
U.S.DEP'T. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)		

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Assistant Examiner	
		Total Claims	Print Claim for O.G.
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drwg.	Figs.Drwg.
TERMINAL		Print Fig.	
DISCLAIMER		Primary Examiner	
		Application Examiner	
PREPARED FOR ISSUE			
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